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# Chip Scale

REVIEW

**EXTRA!**

October 15, 2004

## Packaging Advances Hampered by Lack of Development Money

By Ron Iscoff, Editor

**San Jose**—Although interconnects, not transistors, have become the gating item for improved IC performance, advances in IC assembly and packaging have been hampered due to a lack of funding for development, according to Dr. W.R. "Bill" Bottoms, keynote speaker at the recent International Wafer-Level Packaging Congress.

Dr. Bottoms, chairman and CEO of Third Millennium Test Solutions, noted that billions of dollars has been spent on the development of silicon fabrication and for the development of compound semiconductors, as well.

"Yet, we're in the millions category when we look at what has been spent on the development of technology for assembly and packaging."



Dr. Bottoms observed that today assembly and packaging costs often exceed fab costs, and system performance is dominated by the performance of the interconnects, not by transistor performance. In almost every case, he noted, transistors are not the performance limiter.

An advertisement for Datacon. It features a central image of a hybrid die bonding machine with a blue and white design. To the right is a yellow car. Below the car is a circuit board. A blue starburst graphic contains the text "See us at IMAPS booth 340". The text "the world of advanced packaging" is at the top left. At the bottom, it says "Hybrid Die Bonding Requirements? Keep Pace with Technology from Datacon" and "215-245-3050 • info.dcn@datacon.at". The Datacon logo is at the bottom right.

"Every year, we have to deliver more performance to our customers than we did last year for less money, or the market will get smaller.

"The failure to achieve performance improvements in assembly, packaging and test threaten industry growth."

**(CONTINUED, please click here.)**

## First Int'l Wafer-Level Packaging Congress Ranked a Success



Gilbert Fluetsch of Ismeca, a show exhibitor, talks with SMTA's Kristin Nafstad.

San Jose—The first International Wafer-Level Packaging Congress that concluded a three-day run on October 12, “was a success by any measure,” said Gene Selven, publisher of *Chip Scale Review*, the copresenter of the show with the SMTA.

Originally, Selven noted, the IWLPC prepared for 25 exhibitors. By show time, 47 exhibitors had joined and several had to be turned away.

Additionally, some 46 papers were presented, covering the full spectrum of wafer-level and chip-size/chip-scale packaging assembly, packaging and test issues.

Plans are now underway to finalize the dates for next year's event, which will be held during the fourth quarter.



*Chip Scale Review*'s Terry Thompson discusses the show with SMTA's JoAnn Stromberg.



Exhibitor Dean Smith of Thin Film Engineering chats with Publisher Gene Selven (right).

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Jacques Coderre of Universal Instruments checks with his office during the IWLPC.



Market researchers Sandra Winkler of Electronic Trends and Jim Walker of Gartner Dataquest share their forecasts with Lee Smith (right) of Texas Instruments.



Vern Solberg (left) and Giles Humpston, both of Tessera, San Jose, enjoy a break in the conference.

# More Photos from the IWLPC, San Jose, Oct. 10-12



A visitor stops by the FlipChip International booth to chat with (from left), Jay Hayes, Dr. Haluk Balkan and Jacinta Meilhon.



Doug Stewart of Precision Process Equipment Inc., Niagara Falls, N.Y., was elated with the quality of show visitors.



David Hays of Unitive Electronics (in suit), a new Amkor acquisition, prepares to meet visitors.



Meanwhile, Heather Garonzik of competitor STATS SchipPAC, does likewise.

## PEOPLE: JOEL CAMARDA, PHIL MARCOUX TO NEW POSTS

*San Francisco*—**Joel J. Camarda**, an industry veteran, has left Kulicke & Soffa Industries to form his own consulting firm, Camarda Associates. Camarda, who was earlier at IPAC, San Jose, will provide semiconductor packaging, assembly, operations and manufacturing management consulting. Contact him at [jcamarda@semiops.com](mailto:jcamarda@semiops.com).



*Fremont, Calif.*—**Phil Marcoux**, executive director of trade association MEPTEC, has joined SensArray as “business maker.” He reports to Wayne Renken, president and CEO. He will also maintain his post with MEPTEC. Prior to joining SensArray, Marcoux was vice president of sales and marketing at several firms, including IPAC and Tru-Si. Contact him at [phil\\_marcoux@sensarray.com](mailto:phil_marcoux@sensarray.com)



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## **FLIPCHIP INTERNATIONAL OPENS NEW DESIGN CENTER**

*Phoenix, Ariz.*--**FlipChip International** has opened a Reliability and Design Center for wafer-level packaging and flip-chip bumping within its Phoenix facility.

The center will support FCI's design wins for radio-on-chip, wireless and broadband semiconductor devices employed in next-generation video phones and wireless sensors. [flipchip.com]

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## **PACKAGING ADVANCES** (Continued from Page 1)

However, Dr. Bottoms observed, "The gap has been recognized, and we're beginning to see more innovation in the backend." The most important innovation today, he said, is wafer-level packaging and the associated technologies that are being developed with it.

"Defining WLP is really simple. It's a technology where all the IC packaging is performed at wafer level. If you use that very simplistic definition," he added, "there are certain constraints that go along with it."

### **Die Shrinks**

These constraints include the need for all interconnects to be within the boundaries of the individual die profiles. That requirement, he added, may inhibit the use of WLP for high pincount devices, since the industry practice is to cut costs through die shrinks.

While die shrinks are common to reduce costs, "nobody is shrinking die to improve performance," according to Dr. Bottoms. The limitation on wafer-level packaging is how many I/O can be placed under the chip while still offering an interconnect level that will fit on an expensive substrate.

He reminded the dinner audience at the DoubleTree Hotel, that wafer-level packaging is not a new idea.

The basic infrastructure that allowed chip-scale packaging at the wafer level existed when chip-scale packages were introduced in the 1980s.

"Those of you who just entered the field and think you're at the beginning and get to ride it as it goes along are wrong! Actually, WLP started when the enabling technology was first published in 1961."

The start of WLP, he said, was the publication by Paul Totta of IBM's C4 technology. The basic infrastructure that allowed the building of chip-scale packaging at the wafer level existed when chip-scale packages were introduced in the 1980s.

"Depending on how you look at it, we've had WLP for more than 40 years. If you take a more conservative view, it's been 20 years," Dr. Bottoms noted. "But by any measure, it's been around for a long time!"

He said the first time he saw a claim that a company was shipping WLPs was in 1998.

### **Search Engines**

"I went to the search engines to see what happened to WLP. Both Google and Yahoo say there were significant citations for WLP in 1964. In 1996, we started to see explosive growth (in citations)." By this year, he said, both Google and Yahoo showed a major increase in the number of citations related to WLP.

Prismark Partners, an industry research firm, forecast a five-fold increase in WLP between 2002 and 2007, Dr. Bottoms pointed out. "As we know, they were too conservative; it's going to be more than that."

Dr. Bottoms said, "No matter where you look, you will find that wafer-level packaging, chip-size packaging and innovations in the way we interconnect transistors and make usable devices that fit on PC boards is getting a lot of attention." (Continued below)

## **PACKAGING ADVANCES (Continued)**

That attention, he noted, is why transitions in the electronics industry will be driven in the near term by assembly, packaging and test, rather than by transistor design.

WLP is finally taking off, he said, because it's cheaper than the alternatives for a device that's suited to the technology.

"WLP gives you improved performance: It gives you decreased power so your battery can last longer or your system can run faster. It has a shorter time to market; the process is simplified; the pipeline is shorter. WLP is smaller in size, so it fits the form factor of the kinds of devices we might carry around with us."

Dr. Bottoms said WLP is less expensive because it doesn't use much material. "It's also a simple process, a parallel process." It only requires, he noted, placing a redistribution layer, then putting passivation and encapsulation on top of the redistributed layer. Then the wafer-level package is tested and singulated.

WLP gives you decreased power so your battery can last longer or your system can run faster.

There are cost savings, additionally, because you don't need a test handler, which typically costs more than a wafer prober in the backend. Additionally, there are savings at test. "Instead of testing in probe and testing again in the package, you just test once," Dr. Bottoms said, and you can eliminate final test.

Comparing a leadframe-based device against a wafer-level packaged device, leadframe-based devices cost more as pincounts rise.

There are also performance improvements in wafer-level-packaged devices because signal paths are shorter, inductance is less, and both capacitance and trace resistance are lower. Looking at WLCSP on a per-pin basis versus a Small Outline Package, Dr. Bottoms said electrical performance is better by a factor of two, because of lower inductance, lower noise, lower voltage drop and better signal quality.

### **Shorter Time-to-Market**

Time-to-market with WLPs is shorter, he said, because only one test set, one contactor and one test program have to be developed. "There are also fewer steps in the packaging flow, and the supply chain is shorter."

With all of WLPs attributes, including better performance, "Why did it take 40 years" to hit the mainstream, he asked rhetorically. The answer, he said, is cost. "In the early days," the cost of substrates was too high. Additionally, he noted, test at wafer level still isn't practical except in specialized cases.

Moreover, when using WLP-a build-up technology-you are risking the complete wafer, which in the case of a company like Intel, may be valued at \$100,000. Done conventionally, the risk is only to one layer at a time.

WLP is not on the "ground floor," Dr. Bottoms reminded his audience. "If you want to catch something on the upswing, you might have missed the first 40 years of development; however, you have plenty of time to catch the growth."