3D Silicon & Glass Interposers

August 2012

Sample

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3D integration has been on everybody’s minds for over 5 years throughout the semiconductor industry, and it fast met commercial success for a few applications including MEMS, sensors and power amplifiers. However, past this initial euphoria, and even though technical developments comforted most observers that mass volume adoption of 3D was not out of reach, some technical and supply chain hurdles proved higher than anticipated.

2.5D integration by means of 3D glass or silicon interposers was then exposed by experts as a necessary stepping stone to full 3D integration. In our first report on 3D interposers and 2.5D integration in 2010, after listing the various applications of this technology trend and their drivers, we showed that glass and silicon interposers were expected to become high volume necessities rather just high performance solutions for a few niche applications.

In this 2012 edition of the report, we show more evidence of our findings from 2 years ago: after refining the applications and drivers of 3D interposers and 2.5D integration, thanks to detailed forecasts, Yole Developpement estimates that far from being a stepping stone technology to full 3D integration, 3D interposers and 2.5D integration is emerging as a mass volume long-lasting trend of the semiconductor industry.
What’s new since our 2010 report on interposers?

• In 2010, we started the report by asking « are 3D glass/silicon interposers a myth, a high-end solution for niche applications or a high volume necessity? », and we concluded that it was nothing like a myth, and that it was already entering high volumes for a limited number of applications

• As of 2012, we confirm this conclusion from 2 years ago, especially since we collected many proofpoints: press releases, investments, company packaging roadmaps,… All concur that 3D silicon/glass interposers are becoming a key piece of the 2010-2020 semiconductor technology puzzle

• Drivers by application are now clearer than 2 years ago, which allowed us to accurately forecast the growth of this industry trend.

• First demonstrators have been made in 2011, especially the Xilinx Virtex 7 FPGA, supported by motivated supply chain leaders (TSMC and Amkor), which proved not only feasibility of such complex 2.5D modules, but also their benefits: higher bandwidth, higher integration capacity, lower power consumption, managed thermal dissipation.

• The remaining questions are: how fast and at what, and for which exact applications and through which players is this trend going to succeed? These are the main focus points of this 2012 report.
Recent key press announcements
linked to 2.5D silicon / glass interposer concepts

- Below is a non-exhaustive list of articles related to 2.5D/3D interposers recently published on www.i-micronews.com (Yole’s industry news website)

<table>
<thead>
<tr>
<th>Date</th>
<th>Announcement</th>
</tr>
</thead>
<tbody>
<tr>
<td>2012</td>
<td>Xilinx ships world’s first heterogeneous 3D FPGA using 2.5D silicon interposer</td>
</tr>
<tr>
<td>2012</td>
<td>Are silicon interposers “luxury” solutions?</td>
</tr>
<tr>
<td>2012</td>
<td>2.5D interposers look increasingly like the near term, high performance solution</td>
</tr>
<tr>
<td>2012</td>
<td>UMC’s new 300mm fab to propose leading foundry services for BSI, 2.5D interposer and 3DIC</td>
</tr>
<tr>
<td>2012</td>
<td>Focus on Qualcomm 2.5D Interposer and 3DIC roadmap</td>
</tr>
<tr>
<td>2012</td>
<td>2.5D Interposer and 3DIC seen as innovation enabler!</td>
</tr>
<tr>
<td>2012</td>
<td>2.5D Interposers with stacked FPGA enable silicon convergence</td>
</tr>
<tr>
<td>2012</td>
<td>Altera and TSMC develop heterogeneous 3DIC test vehicle with 2.5D Interposer</td>
</tr>
<tr>
<td>2012</td>
<td>AGC reveals high speed drilling technology for 2.5D glass interposer</td>
</tr>
<tr>
<td>2012</td>
<td>IBM demonstrate voltage regulator integration on 2.5D silicon interposer platform</td>
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<tr>
<td>2011</td>
<td>TSMC and Arteris to develop 2.5 silicon-interposer-based NOCs</td>
</tr>
<tr>
<td>2011</td>
<td>SiBDI to commercialize Silicon interposer HB-LED submount</td>
</tr>
<tr>
<td>2011</td>
<td>VisEra enters LED lighting sector with silicon wafer level package interposer</td>
</tr>
<tr>
<td>2011</td>
<td>CEA-LETI &amp; Shinko to partner on Silicon interposers development</td>
</tr>
<tr>
<td>2011</td>
<td>A*STAR and Tezzaron to develop 2.5D &amp; 3D Silicon Interposers</td>
</tr>
<tr>
<td>2011</td>
<td>TSMC latest developments on TSV and Silicon Interposer</td>
</tr>
<tr>
<td>2011</td>
<td>2.5D interposers: a closer look</td>
</tr>
<tr>
<td>2011</td>
<td>Xilinx 2.5D FPGA’s coming off the production line: a closer look</td>
</tr>
<tr>
<td>2011</td>
<td>Betting on through silicon vias in glass substrates</td>
</tr>
<tr>
<td>2011</td>
<td>Through-Silicon via supplier ALLVIA attains ITAR registration</td>
</tr>
<tr>
<td>2011</td>
<td>Xilinx and Amkor discuss 3D interposer programs</td>
</tr>
<tr>
<td>2011</td>
<td>IME &amp; Elta Systems to develop TSV silicon interposers for Power Amplifier applications</td>
</tr>
<tr>
<td>2011</td>
<td>PlanOptik presents holed Glass carrier substrate for Thin wafer Handling of TSV wafers</td>
</tr>
<tr>
<td>2010</td>
<td>IBM &amp; Semtech team up for 3D TSV interposers</td>
</tr>
<tr>
<td>2010</td>
<td>ALLVIA to present advanced logic applications for silicon interposers</td>
</tr>
<tr>
<td>2010</td>
<td>NEPES silicon interposer module contains IPD and TSV</td>
</tr>
<tr>
<td>2010</td>
<td>Xilinx brings 3D TSV interconnects to commercialization phase in digital FPGA world</td>
</tr>
<tr>
<td>2010</td>
<td>Why the secrecy surrounding TSI development?</td>
</tr>
<tr>
<td>2010</td>
<td>TSMC reveals plan for 3DIC designs based on Silicon interposers &amp; TSV</td>
</tr>
<tr>
<td>2010</td>
<td>ALLVIA integrates Thin-film IPD capacitors in Silicon interposers</td>
</tr>
<tr>
<td>2010</td>
<td>ASE gears up for 2.5D, 3D IC commercialization</td>
</tr>
<tr>
<td>2010</td>
<td>IPDIA opens multi-parties 3D TSV Silicon Interposer Program</td>
</tr>
<tr>
<td>2010</td>
<td>ALLVIA completes reliability testing of silicon interposer for stacked semiconductors</td>
</tr>
<tr>
<td>2009</td>
<td>TSV foundry ALLVIA &amp; SunSil ready to commercialize 3D Silicon interposers</td>
</tr>
<tr>
<td>2009</td>
<td>R&amp;D Consortium readies for Low Cost WLP of Silicon Interposers</td>
</tr>
<tr>
<td>2008</td>
<td>Silicon Interposers Wait for an Application</td>
</tr>
<tr>
<td>2008</td>
<td>New 3D-consortium formed focusing on Si-interposer technologies</td>
</tr>
</tbody>
</table>
Choosing between 2.5D & 3D

- 2.5D « system partitioning » interposers will be used in the long term for those applications which cannot go the full 3D integration way due to high power losses of the logic die, neighboring and thus affecting the memory ICs

<table>
<thead>
<tr>
<th></th>
<th>several standard packages</th>
<th>2.5D SiP</th>
<th>3D SiP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology and infrastructure</td>
<td>+</td>
<td>-</td>
<td>--</td>
</tr>
<tr>
<td>maturity as of Q3 2012</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Electrical bandwidth</td>
<td>-</td>
<td>+</td>
<td>++</td>
</tr>
<tr>
<td>Power consumption</td>
<td>-</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>Heterogeneous integration</td>
<td>-</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>Size</td>
<td>-</td>
<td>+</td>
<td>++</td>
</tr>
<tr>
<td>Thermal Management</td>
<td>++</td>
<td>+</td>
<td>-</td>
</tr>
</tbody>
</table>
We identified the following technology segments for 3D interposers:
- MEMS and sensors 3D capping interposers
- “System partitioning” interposers
- Interposers for CMOS image sensors
- 3D LED silicon substrates
- 3D Integrated Passive Devices (IPDs)
- Miscellaneous interposers
2.5D interposer solution for Large die Logic applications (FPGA, ASICs, DSP, etc…)

- Several ‘slices’ instead of one die: 3D-SOC re-partionned logic design
  - Increase CMOS manufacturing yield (because of smaller die size)
  - High density wiring at the surface of the 4 layer copper damascene silicon interposer wafer
    \(\rightarrow\) breakthrough in COST versus POWER CONSUMPTION versus PERFORMANCE

X100 high density wiring interface! (w.r.t. organic interposer)

Silicon interposer \(\rightarrow\) BGA Laminate

PCB
## Logic + memory integration: competing solutions

<table>
<thead>
<tr>
<th><strong>Pros</strong></th>
<th><strong>Cons</strong></th>
<th><strong>Apps</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PoP</strong></td>
<td><strong>2.5D with Interposer</strong></td>
<td><strong>3D</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Clear cost ownership: bottom package belongs to logic manufacturer, top package goes to memory manufacturer, 3D integration by OEM</td>
<td>• Package height</td>
<td>Baseband ICs</td>
</tr>
<tr>
<td></td>
<td>• Flexible sourcing of DRAM</td>
<td>Networking &amp; storage ASICS, CPU, GPU</td>
</tr>
<tr>
<td></td>
<td>• Flexible test of each separate stack</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Application Processors for tablets &amp; smartphones</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Short DRAM to Logic interconnections for high frequency memory access</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Wide IO interface for memory access with high bandwidth</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Low package height</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Thermal management</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Very short interconnections DRAM to logic</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Very wide IO interface for high bandwidth memory access</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• No DRAM sourcing flexibility before IO standardization</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Thermal management: heat propagation logic to DRAM</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Cost of RDL on DRAM (before standardization)</td>
<td></td>
</tr>
</tbody>
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Example of performance driven 2.5D integration

**GPU for gaming**

- Sony PS4 (to be released for the 2013 holiday season or in 2014) will have a GPU on interposer with a 512-wide data bus and on interposer memory
- Will probably be an AMD chip
- Future gaming platforms will offer 3D imagery, which requires fast & high bandwidth computing power.
- 2.5D is unanimously praised as the solution for this purpose
- “GPU-RAM Bandwidth is the key factor for rendering performance” – Sept 2011, Teiji Yutaka, SVP Technology Platform, Sony Computer Entertainment

An interposer module for (Yole assumption) an AMD GPU demonstrator
 Courtesy of Global Foundries, 2012
2 types of interposers

**Fine-pitch Interposers**

- High-end and high power logic applications (GPU/CPU/FPGA/ASIC)
  - Performance (bandwidth & energy consumption) driven
  - thin (50-100µm) & fine-pitch (via diameter 10-15µm), microbumping below 50µm
  - Fine line.spacing below 3µm/3µm
  - Manufactured by CMOS foundries on 300mm silicon wafers with design rules close to the back-end-of-line (BEOL) of CMOS 65nm

**Coarse Interposers**

- Analogue/MEMS/Sensors/Lighting
  - Size and cost driven
  - Any thickness: 20µm to 500µm, large via diameter (30µm-500µm)
  - Line.spacing above 3µm/3µm
  - Manufactured by MEMS foundries or OSATs or IDMs or glass manufacturers on glass or silicon wafers or panels
Coarse versus Fine-pitch Interposers
characteristics As of 2012

<table>
<thead>
<tr>
<th>Substrate material</th>
<th>silicon</th>
<th>glass</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate thickness</td>
<td>thin 20µm</td>
<td>thick 200µm</td>
</tr>
<tr>
<td>wafer size</td>
<td>6 inch</td>
<td>8 inch</td>
</tr>
<tr>
<td>Amount of front side routing metal layers</td>
<td>1ML</td>
<td>2ML</td>
</tr>
<tr>
<td>Amount of back side routing metal layers</td>
<td>0ML</td>
<td>1ML</td>
</tr>
<tr>
<td>Line width/spacing</td>
<td>1µm/1µm</td>
<td>5µm/5µm</td>
</tr>
<tr>
<td>Line thickness upper layer</td>
<td>0.5µm</td>
<td>1µm</td>
</tr>
<tr>
<td>Planarization of metal layers</td>
<td>CMP (copper damascene)</td>
<td>No planarization</td>
</tr>
<tr>
<td>Via pitch</td>
<td>20µm</td>
<td>50µm</td>
</tr>
<tr>
<td>Die size</td>
<td>1x1mm²</td>
<td>5x5mm²</td>
</tr>
<tr>
<td>Provider</td>
<td>IC wafer foundry</td>
<td>OSAT/MEMS/WLP foundry</td>
</tr>
</tbody>
</table>

We generally consider that there technically are 2 types of interposers:

- **Fine-pitch interposers** for high-end and high power logic applications (GPU/CPU/FPGA/ASIC)
  - They feature fine geometries down to 1µm
  - They are manufactured by IC wafer foundries (on CMOS 65nm 300mm diameter type of wafers)
  - Dies are generally larger (larger than 100mm²)

- **Coarse interposers** for Analogue/MEMS/Sensors/Lighting
  - They feature larger geometries
  - They are manufactured by OSATs, glass suppliers or WLP foundries
# 3D silicon/glass interposers

**Who is doing what? Main players**

<table>
<thead>
<tr>
<th>Wafer/panel supply</th>
<th>TSV/TGV making</th>
<th>RDL</th>
<th>test of interposer</th>
<th>Bumping</th>
<th>Packaging and assembly</th>
<th>final test</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon substrate makers</td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>Glass substrate makers</td>
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<tr>
<td>IC wafer foundry</td>
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<tr>
<td>MEMS wafer foundry (or IPD wafer foundry)</td>
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<td></td>
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<tr>
<td>OSATs</td>
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<td></td>
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<tr>
<td>PCB manufacturers</td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>IDMs</td>
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</tbody>
</table>

**Silicon substrate makers**
- New TSMC model

**Glass substrate makers**
- HOYA

**IC wafer foundry**
- GLOBAL FOUNDRIES
- UMC

**MEMS wafer foundry (or IPD wafer foundry)**
- DALSA
- Silex Microsystems
- IMT

**OSATs**
- STATSChipPAC
- Amkor Technology
- STATSChipPAC
- Powertech Technology Inc.
- Amkor Technology
- SPIL

**PCB manufacturers**
- SHINKO
- TBI IBIDEN CO., LTD.

**IDMs**
- Intel
- ST
- Samsung
Yole’s Market Forecasting Methodology

- Yole’s market forecasting methodology is based on the “top-down meets bottom-up” analyses
  - 2 complementary analyses are carried out and cross-checked:
    - The top-down analysis derives the wafer forecasts from an analysis of the end products where 2.5D interposers are expected, application by application, taking into account the penetration rate of the technology for each product type, as well as their yields and die sizes.
    - The bottom-up analysis is based on the evaluation of the worldwide production capacity evaluated through interviews of industry players (foundries, OSATs, equipment and material makers) and company revenue reports.

Throughout the following market forecast slides, we show forecasts from our top-down analysis, followed by the 2011 status of the processed interposer wafers through our bottom-up analysis.
Interposers revenues within the context of IC Packaging substrates

Another way of looking at 2.5D expected revenues is – even if arguably – to compare them to the wide established market of IC Packaging substrates: after all, 2.5D/3D interposers are just another layer of vertical and horizontal interconnections inside the package.

This comparison speaks for itself: as of 2017, Yole expects the 2.5D/3D interposer revenues to reach 15% of the packaging substrate market value.
2.5D/3D interposer 2010-2017 wafer forecasts
breakdown by end product

2.5D Interposer demand forecast
Breakdown by end product (12” eq. wafers)

- Base stations
- HPC
- Server
- Automotive: Total
- Set-Top Box and Hybrid Set-Top Box
- OTHER
- Data Center
- Desktop PC
- General Lighting (LED Packages)
- Network (Switch, Router, Appliance)
- Smart TV
- Laptop
- Game Station Controller
- Tablet
- Game stations
- Mobile Phone

*Other = Missile, Machine Vision, Helicopter, Drone, Defense UAV, Civil UAV, Drilling systems, Guided munitions, Professional imaging, Infantry gear, Camera pill, Implantable CRM, Camcorder, Hearing aids, ATE, Trucks, Buses, PMP, MP3, PND, DSC, SLR, Femtocell, 3G Dongle
2.5D/3D interposer wafer demand forecast in 2017

Top 20 of end application (12''eq.wafers)

- **Television Set**: 250 705 wafers (12''eq.) 10%
- **Set-Top Box and Hybrid Set Top Box**: 294 121 wafers (12''eq.) 11%
- **Game stations**: 025 wafers (12''eq.) 11%
- **Tablet**: 302 701 wafers (12''eq.) 12%
- **Game Station Controller**: 217 023 wafers (12''eq.) 8%
- **General Lighting (LED Packages)**: 206 535 wafers (12''eq.) 8%
- **Network (Switch, Router, Appliance)**: 143 819 wafers (12''eq.) 5%
- **Data Center**: 10 896 wafers (12''eq.) 0%
- **Base stations**: 8 507 wafers (12''eq.) 0%
- **Mobile Phone**: 418 567 wafers (12''eq.) 16%
- **Other Applications**: 127 408 wafers (12''eq.) 5%
- **HPC**: 70 298 wafers (12''eq.) 3%
- **Desktop PC**: 66 654 wafers (12''eq.) 3%
- **Laptop**: 102 333 wafers (12''eq.) 4%
- **Automotive**: Total 76 678 wafers (12''eq.) 3%
- **Game stations**: 025 wafers (12''eq.) 11%

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Presentation of Yole’s activities
Yole Développement activity & services

- Yole Développement provides powerfull tools and services...
  - Strategic analysis
  - Technology evaluation
  - Market Research & Marketing analysis
  - Specific services for investors by Yole Finance

- ...In 6 high technology areas
  - MEMS
  - Photovoltaic
  - Microfluidics
  - Advanced packaging
  - Power electronics
  - Compound semiconductors
Yole activities in Advanced Packaging

- Market Research Reports
- Strategy Consulting services

Media business
News feed / Magazines / Webcasts

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NEW service: IP analysis

Phase II depends on Phase I results. Phase III depends on phase II results.
About Yole’s Advanced Packaging Analysts team (1/2)

Jerome Baron
- Jerome is the business unit manager of the semiconductor packaging market research at Yole Développement. He has been following the 3D packaging market evolution since its early beginnings at the device, equipment and material levels. He was granted a Master of Science degree from INSA-Lyon in France as well as a Master of Research from INL – Lyon Institute of Nanotechnology.

Contact: baron@yole.fr

Phil Garrou
- Phil recently joined Yole Développement forces as senior technical advisor in the fields of advanced packaging. Phil has more than 20 years extensive experiences in the semiconductor industry where he mainly served as global marketing manager for DOW Chemical’s BCB polymer business.

Contact: garrou@yole.fr

Lionel Cadix
- Lionel joined Yole after the completion of several projects linked to the characterization and modeling of high density TSV and 3DIC chip stacking in collaboration with CEA-Leti and STMicroelectronics during his PhD. He is author of several publications and 8 patents in the field of 3D Integration.

Contact: cadix@yole.fr

Jean-Marc Yannou
- Jean-Marc joined Yole Développement as technology and market expert in the fields of advanced packaging and Integrated Passive Devices. He has 15-years of experience in the semiconductor industry. He worked for Texas Instruments & NXP semiconductors where he was Innovation Manager for System-in-Package technologies.

Contact: yannou@yole.fr
Amandine Pizzagalli

– Amandine recently joined Yole Development Advanced Packaging and MEMS manufacturing teams after graduating as an engineer in Electronics, with a specialization in Semiconductors and Nano Electronics Technologies. She worked in the past for Air Liquide with an emphasis on CVD and ALD processes for semiconductor applications

Contact: pizzagalli@yole.fr

Eric Mounier

– Dr. Eric Mounier co-founded Yole Developpement in 1998. He is in charge of technology analysis for MEMS related manufacturing technologies within the company. In the 3D Packaging area, Eric has developed a unique Cost modeling tool “TSV+” able to simulate the cost of ownership of several different Through-Silicon-Vias and 3D integration scenarios

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